

In the Claims:

1. (Previously presented) A Phase Locked Loop, for synchronization of a clock signal with an incoming data signal, comprising
a frequency detector including
an unbalanced quadricorrelator, the quadricorrelator including
a first multiplexer,
a second multiplexer, and
double edge clocked bi-stable circuits, supplied by incoming mutually quadrature phase shifted signals and coupled to the first multiplexer and to the second multiplexer, the first and second multiplexers controlled by a signal having a same bitrate as the incoming signal;
a first phase detector that includes a D flip flop that receives, as a data input, a first signal pair provided by the first multiplexer and that is clocked by a second signal pair provided by the second multiplexer;
a first transistor pair receiving the second signal pair on respective gates for determining a state ON or OFF of a current through the first transistor pair;
and
a second transistor pair biased by current through the first transistor pair and receiving the first signal pair and generating an output signal indicative for a frequency error between the incoming data signal and the clock signal.
2. (Previously presented) A Phase Locked Loop as claimed in claim 1, wherein the frequency detector comprises a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer, and a second pair of double edge clocked bi-stable circuits coupled to the second multiplexer, wherein the first and second pairs of bi-stable circuits are supplied by mutually quadrature phase shifted signals respectively to provide the first signal pair and the second signal pair indicative for a phase difference between the incoming signal and the mutually quadrature phase shifted signals.

3. (Cancelled).
4. (Cancelled)
5. (Previously presented) A Phase Locked Loop as claimed in claim 2, further including a voltage controlled oscillator wherein the mutually quadrature phase shifted signals are generated by the voltage controlled oscillator.
6. (Previously presented) A Phase Locked Loop as claimed in 5, further including an adder;
a first charge pump; and
a first low-pass filter,
wherein a frequency error signal produced by the quadricorrelator is inputted to a coarse control input of the voltage controlled oscillator via the first charge pump coupled to the first low-pass filter coupled to the adder.
7. (Previously presented) A Phase Locked Loop, for synchronization with an incoming data signal, comprising
a voltage controlled oscillator generating mutually quadrature phase shifted signals,
a frequency detector including an unbalanced quadricorrelator, the quadricorrelator including
a first multiplexer,
a second multiplexer,
a first pair of double edge clocked bi-stable circuits,
a second pair of double edge clocked bi-stable circuits,
wherein the first pair and the second pair of double edge clocked bi-stable circuits are supplied by the mutually quadrature phase shifted signals,
respectively, to provide a first signal pair and a second signal pair indicative of a phase difference between the incoming data signal and the mutually quadrature phase shifted signals, and

- a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer;
- a first low-pass filter;
- a second low-pass filter;
- an adder;
- a first charge pump for inputting a coarse control input for the voltage controlled oscillator using a frequency error signal produced by the quadricorrelator and coupled to the first low-pass filter and to the adder;
- a second charge pump; and
- a further phase detector;

wherein a fine control input is controlled by a signal provided by the further phase detector coupled to the second charge pump coupled to the second low-pass filter.

8. (Previously presented) A Phase Locked Loop, for use with an incoming data signal, comprising:

- a voltage controlled oscillator having a coarse control input and a fine control input and generating mutually quadrature phase-shifted signals;
- a first charge pump;
- a second charge pump;
- a first low-pass filter;
- a second low-pass filter;
- an adder;
- a quadricorrelator generating a frequency error signal inputted to the coarse control input of the voltage controlled oscillator via the first charge pump coupled to the first low-pass filter coupled to the adder, the quadricorrelator including
 - a frequency detector including
 - a first multiplexer,
 - a second multiplexer,
 - a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer and

a second pair of double edge clocked bi-stable circuits coupled to the second multiplexer to provide a second signal pair, the first and second pairs of bi-stable circuits being supplied by the mutually quadrature phase shifted signals, the first and second multiplexers being controlled by a signal having a same bitrate as the incoming signal and respectively providing a first signal pair and a second signal pair indicative for a phase difference between an incoming signal and the mutually quadrature phase shifted signals;
a transistor pair; and
a phase detector controlled by the first signal pair and the second signal pair, the phase detector including

a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of the transistor pair for determining a state ON or OFF of a current through said transistor pair; and

a second phase detector generating a phase error inputted to the fine control input of the voltage controlled oscillator via the second charge pump coupled to the second low-pass filter.

9. (Previously presented) The Phase Locked Loop of claim 8, further including a third low-pass filter, wherein the phase error is further inputted to the coarse control input of the voltage controlled oscillator via the second charge pump coupled to the third low-pass filter coupled to the adder.